# EEO 366: Design using Programmable Mixed-Signal Systems-on-Chip

Spring 2016

**2015-2016 Catalog Description:**
The course presents state-of-the-art concepts and techniques for design of embedded systems consisting of analog, hardware and software components. Discussed topics include system modeling and specification, architectures for embedded mixed-signal systems, performance evaluation, and system optimization. The course follows the top-down design paradigm based on IP cores. Course requirements include three reports on system specification and various co-design tasks.

**Course Designation:** Elective
**Course Credits**: 4
**Text Books:** A. Doboli, E. Currie, "Introduction to Mixed-Signal Embedded Design", Springer, 2010.

**Prerequisites**: None.

**Coordinator: Dr. Alex Doboli**

**Goals:**
Upon completion of the course, students will possess knowledge about state-of-the-art methodologies and techniques for hardware/software co-design of embedded systems. They will be able to (1) develop system-level specifications using high-level languages, (2) model system performance, and (3) implement algorithms for co-design.

**Covered Topics**:
1) **Introduction to Co-Design**:
   a. Problem description, goals of co-design, co-design steps, existing co-design approaches, and present challenges.
2) **System Modeling and Specification**:
   a. Models of computation (Signal flow graphs, Data flow model, Task graphs, Finite State Machines, hierarchical models).
3) **Architectures for Embedded Systems**:
   a. Single processor – coprocessor architecture, mixed-signal architectures, multiprocessor architectures, reconfigurable architectures, Systems on Chip.

4) **Performance Modeling**:
   a. System-level performance modeling vs. low-level performance modeling.
   b. Modeling of system latency, energy consumption etc for hardware and software.
   c. Modeling of analog and mixed-signal systems.
   d. Estimation of memory requirements.

5) **System-Level Synthesis and Trade-off Analysis**:
   a. Design of customized digital and analog blocks.
   b. Hardware/software partitioning. Task binding.
   c. IP core integration and communication synthesis: Hardware and software interface synthesis.
   d. Hardware IP core synthesis: High-level synthesis: behavioral specification of hardware, module set allocation, resource binding, operation scheduling, controller design.

**Class/laboratory Schedule: Lecture: 1hr 20min/2 days per week**
**Lab: 3 hr/1 day per week**

| Program Outcomes | % contribution* |
|---|---|
| ❑ (a) an ability to apply knowledge of mathematics, science and engineering | |
| X❑ (b1) an ability to design and conduct experiments | 10% |
| X❑ (b2) an ability to analyze and interpret data | 10% |
| X❑ (c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability | 50% |
| ❑ (d) an ability to function on multi-disciplinary teams | |
| X❑ (e) an ability to identify, formulate, and solve engineering problems | |
| ❑ (f) an understanding of professional and ethical responsibility | |
| X❑ (g) an ability to communicate effectively | 10% |
| ❑ (h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context | |
| ❑ (i) a recognition of the need for, and an ability to engage in life-long learning | |
| ❑ (j) a knowledge of contemporary issues | |
| X❑ (k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice | 20% |
| ❑ Any other outcomes and assessments? | |

* Assume that the total contribution of any course will be 100%. Use the right hand column to indicate the approximate percent that the left hand columns contribute to the overall course.

**Document Prepared by: Dr. Alex Doboli** **Date: 05/12/2017**