

Syllabus - ESE 382 Digital Design Using VHDL and PLDs

K. Short, Spring 19, revised February 2, 2019 4:35 pm

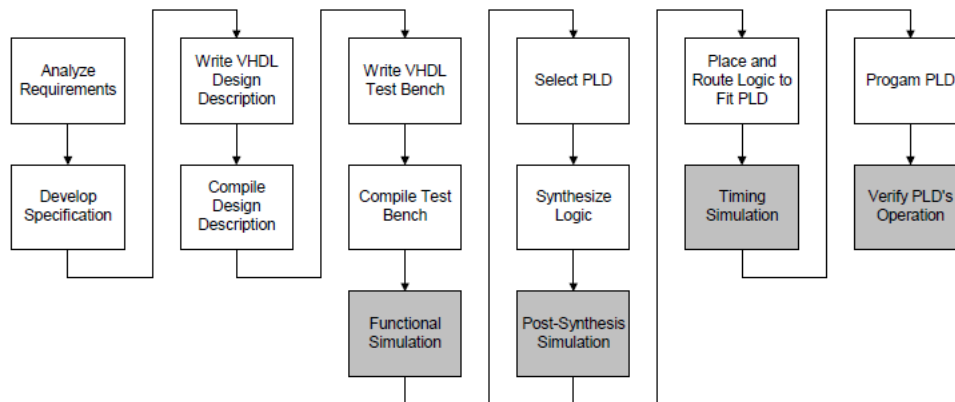
Lecture: Tu. and Thur., 2:30 to 3:50 in room 145 Engineering building.

Office Hours: Tu. and Thur., 4:00 - 6:00 pm, Light Engineering building room 229.

Modern design methodologies allow complex digital systems to be rapidly designed, verified, and implemented using a hardware description language and programmable ICs. The key elements in these methodologies are:

1. Use of a hardware description language (HDL) to describe (model) the system.
2. Use of a software simulator to functionally verify the HDL description.
3. Use of a synthesizer software tool to synthesize a gate-level representation from the HDL description.
4. Use of a place-and-route software tool to map the synthesized logic to a programmable logic device (PLD).
5. Use of a simulator to verify the timing of the synthesized logic mapped to the target PLD.
6. Use of a high logic capacity PLD for immediate implementation of the system.

This design methodology is illustrated by the following diagram.



Expertise in design using an HDL is a critical requirement for digital designers. The most popular hardware description language is VHDL (Very high speed integrated circuit Hardware Description Language). The designer writes a description of the desired system in VHDL. The designer also writes a testbench in VHDL. During simulation, the testbench provides stimulus to the design description's inputs and verifies its outputs.

Using the testbench, the VHDL design description is simulated to verify that the system, as described, meets its functional specification. Then, a VHDL synthesizer and a place and route tool are used to create two files. One file is a VHDL timing model of the synthesized logic fitted to the target PLD. This model is simulated to verify that the design will meet the system's timing requirements. The other file is a configuration file used to program the target PLD.

Course Objectives

The primary course objectives are for you to:

1. Strengthen and extend your understanding of the theory and fundamentals of digital system design.
2. Learn the hardware description language VHDL.
3. Become proficient in a design methodology that uses VHDL to create and verify digital systems that are implemented using PLDs.
4. Learn the basic architecture and operation of various PLDs: including SPLDs, CPLDs, and FPGAs.

Prerequisite

The prerequisite for this course is ESE 218 Digital System Design.

Course Material:

1. The required text for this course is *VHDL for Engineers* by Kenneth L. Short, copyright 2009 by Pearson Education, Inc.
2. Data sheets and other written material, including lecture notes and laboratory assignments are provided on Blackboard.

Digital System Rapid Prototyping (DSRP) Laboratory

Each week, during your assigned three hour laboratory session, you will implement a design in the DSRP Laboratory (room 228 Light Engineering building). Prior to each of your laboratory sessions, you will write and simulate your VHDL code for the design. Simulations can be performed using the free student version of the Aldec simulator software (download from <https://www.aldec.com/students/student.php?id=9>) or use the Aldec simulator in the ECE CAD Laboratory (room 281 Light Engineering building).

In the DSRP Laboratory, you will use a synthesizer and a place-and-route tool to produce a VHDL timing model of your design and a configuration file for programming a PLD. Using the timing model, you will perform a timing simulation of your design. After the timing simulation, you will program a PLD and verify that your design meets the system requirements. ***Laboratory sessions start the week beginning February 3rd.***

The laboratory sections are:

| | | | |
|---------|----|---------------|---------------------|
| Lab L01 | W | 09:00-12:00pm | Light Engr. Lab 228 |
| Lab L02 | W | 02:30-05:30pm | Light Engr. Lab 228 |
| Lab L03 | Th | 10:00-01:00pm | Light Engr. Lab 228 |
| Lab L04 | F | 10:00-01:00pm | Light Engr. Lab 228 |

Grades

Course grades are based on:

| | |
|---|-----|
| Exams (3) | 60% |
| Laboratories (once a week, three hours) | 40% |

The tentative exam dates are:

- Exam 1 - March 5th (Tuesday)
- Exam 2 - April 2nd (Tuesday)
- Exam 3 - April 30th (Tuesday)

Your lowest lab, excluding the last five labs, will be dropped from your lab average.

DUE TO RESOURCE CONSTRAINTS, NO MAKE-UP EXAMS OR MAKE-UP LABORATORIES ARE PROVIDED.

Academic Dishonesty

Academic dishonesty is taken very seriously in this course. If you are caught cheating on an exam you will get a grade of F for the course and your case will be submitted to the Committee on Academic Standing and Appeals (CASA) of the College of Engineering for further action.

Tentative Lecture Schedule

The lectures are presented based on the assumption that you have completed the assigned reading prior to each lecture. This same assumption applies to exams as well. A tentative schedule of the lecture topics is provided on Blackboard. A lecture handout will be available on Blackboard at least one week prior to each lecture. It is recommended that you print this handout and bring it to lecture. The intention is to cover approximately one chapter of the text each week. A more detailed schedule will be provided on Blackboard.

Computers and Other Electronic Devices in Lecture

The use of any type of computing or other electronic devices (including cell phones) by students during lecture is not permitted. These devices must be turned off and put away during lecture.

Blackboard

You can access class information on-line at: <http://blackboard.stonybrook.edu> If you used Blackboard during the Fall semester, your login information (Username and Password) has not changed. If you have never used Stony Brook's Blackboard system, your initial password is your SOLAR ID# and your username is the same as your Stony Brook username, which is generally your first initial and the first 7 letters of your last name.

For problems logging in, go to the helpdesk in the Main Library SINC Site or the Union SINC Site, you can also call: 631-632-9602 or e-mail: helpme@stonybrook.edu.

The following statements are included at the request of the Provost Office.

Disability Support Services (DSS)

If you have a physical, psychological, medical or learning disability that may impact on your ability to carry out assigned course work, you are urged to contact the staff in the Disabled Student Services office (DSS), Room 133 Humanities, 632-6748/TDD. DSS will review your concerns and determine, with you, what accommodations are necessary and appropriate. All information and documentation is confidential.

Academic Integrity Statement

Each student must pursue his or her academic goals honestly and be personally accountable for all submitted work. Representing another person's work as your own is always wrong. Faculty are required to report any suspected instances of academic dishonesty to the Academic Judiciary. Faculty in the Health Sciences Center (School of Health Technology & Management, Nursing, Social Welfare, Dental Medicine) and School of Medicine are required to follow their school-specific procedures. For more comprehensive information on academic integrity, including categories of academic dishonesty, please refer to the academic judiciary website at <http://www.stonybrook.edu/uaa/academicjudiciary/>.

Critical Incident Management

Stony Brook University expects students to respect the rights, privileges, and property of other people. Faculty are required to report to the Office of Judicial Affairs any disruptive behavior that interrupts their ability to teach, compromises the safety of the learning environment, or inhibits students' ability to learn. Faculty in the HSC Schools and the School of Medicine are required to follow their school-specific procedures.